

CLAIMS

What is claimed is:

- Sub 1
2A
1. An apparatus for controlling cell traffic in a switch platform, the apparatus comprising at least one bidirectional first-in-first-out (FIFO) unit, wherein each bidirectional FIFO unit comprises a first and a second unidirectional FIFO buffer, wherein a cell size of the first and second unidirectional FIFO buffers is programmable.
- SUB 1
2
2. The apparatus of claim 1, wherein the first and second unidirectional FIFO buffers each comprise asynchronous read and write ports.
- SUB 1
2
3. The apparatus of claim 1, wherein a word size of the first and second unidirectional FIFO buffers is programmable.
- SUB 1
2
4. The apparatus of claim 1, wherein the at least one bidirectional FIFO unit is coupled to write at least one cell from and read at least one cell to at least one asynchronous transfer mode (ATM) interface, at least one frame relay interface, at least one voice interface, and at least one data interface.
- 1
5. The apparatus of claim 1, wherein the first unidirectional FIFO buffer is coupled to write at least one cell from an ATM interface.
- 2
- 1
6. The apparatus of claim 1, wherein the first unidirectional FIFO buffer is coupled to write at least one cell from a frame relay interface.
- 2

1 7. The apparatus of claim 1, wherein the first unidirectional FIFO buffer is
2 coupled to write at least one cell from a voice interface.

1 8. The apparatus of claim 1, wherein the first unidirectional FIFO buffer is
2 coupled to write at least one cell from a data interface.

1 9. The apparatus of claim 1, wherein the first unidirectional FIFO buffer is
2 coupled to read at least one cell to at least one switch, wherein the at least one
3 switch handles cells from sources having a plurality of bandwidths.

1 10. The apparatus of claim 9, wherein the at least one switch is coupled to
2 route the at least one cell to an OC12 trunk line and to at least one service
3 module.

1 11. The apparatus of claim 10, wherein the at least one service module is
2 coupled to provide the at least one cell to at least one service subscriber using
3 T1, E1, T3, E3, OC3, and OC 12 ports.

1 12. The apparatus of claim 1, wherein the second unidirectional FIFO
2 buffer is coupled to read at least one cell to an ATM interface.

1 13. The apparatus of claim 1, wherein the second unidirectional FIFO
2 buffer is coupled to read at least one cell to a frame relay interface.

1 14. The apparatus of claim 1, wherein the second unidirectional FIFO
2 buffer is coupled to read at least one cell to a voice interface.

1 15. The apparatus of claim 1, wherein the second unidirectional FIFO
2 buffer is coupled to read at least one cell to a data interface.

1 16. The apparatus of claim 1, wherein the second unidirectional FIFO
2 buffer is coupled to write at least one cell from at least one switch, wherein
3 the at least one switch handles cells from sources having a plurality of
4 bandwidths.

1 17. The apparatus of claim 16, wherein the at least one switch is coupled to
2 route the at least one cell from an OC12 trunk line and from at least one
3 service module.

1 18. The apparatus of claim 17, wherein the at least one service module is
2 coupled to provide the at least one cell to at least one service subscriber using
3 T1, E1, T3, E3, OC3, and OC 12 ports.

1 19. The apparatus of claim 1, wherein the at least one bidirectional FIFO
2 unit comprises a diagnostic interface, wherein the diagnostic interface
3 supports a non-destructive read of the at least one bidirectional FIFO unit
4 while at least one cell is being written to and read from the at least one
5 bidirectional FIFO unit.

1 20. The apparatus of claim 1, wherein the at least one cell is written to the
2 second unidirectional FIFO buffer from the first unidirectional FIFO buffer
3 over a first enabled diagnostic loop.

1 21. The apparatus of claim 1, wherein the at least one cell is written to the
2 first unidirectional FIFO buffer from the second unidirectional FIFO buffer
3 over a second enabled diagnostic loop.

1 22. The apparatus of claim 1, wherein each unidirectional FIFO buffer
2 outputs a write port cell count, wherein a write port of each unidirectional
3 FIFO buffer outputs a status indicating space available in the unidirectional
4 FIFO buffer for at least one more cell.

1 23. The apparatus of claim 22, wherein at least one master bidirectional
2 FIFO unit ceases reading at least one cell to a unidirectional FIFO buffer of at
3 least one slave bidirectional FIFO unit in response to the write port cell count,
4 wherein the at least one master bidirectional FIFO unit disables at least one
5 switch from routing at least one cell to the at least one slave bidirectional
6 FIFO unit in response to the write port cell count, wherein the at least one
7 switch routes the at least one cell to another of the at least one slave
8 bidirectional FIFO units in response to the write port cell count.

1 24. The apparatus of claim 23, wherein the at least one master bidirectional
2 FIFO unit resumes reading the at least one cell to the second unidirectional
3 FIFO buffer of the at least one slave bidirectional FIFO unit in response to the
4 write port cell count, wherein the at least one master bidirectional FIFO unit
5 enables at least one switch to route at least one cell to the at least one slave
6 bidirectional FIFO unit in response to the write port cell count.

1 25. The apparatus of claim 1, wherein each unidirectional FIFO buffer
2 outputs a read port cell count, wherein a read port of each unidirectional FIFO

A2 Cont.

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SUB E¹

~~the writer~~

with

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tz.

with

DATE	DESCRIPTION	AMOUNT	BALANCE	DATE	DESCRIPTION	AMOUNT	BALANCE
1900	Jan 1			1901	Jan 1		
1902	Jan 1			1903	Jan 1		
1904	Jan 1			1905	Jan 1		
1906	Jan 1			1907	Jan 1		
1908	Jan 1			1909	Jan 1		
1910	Jan 1			1911	Jan 1		
1912	Jan 1			1913	Jan 1		
1914	Jan 1			1915	Jan 1		
1916	Jan 1			1917	Jan 1		
1918	Jan 1			1919	Jan 1		
1920	Jan 1			1921	Jan 1		
1922	Jan 1			1923	Jan 1		
1924	Jan 1			1925	Jan 1		
1926	Jan 1			1927	Jan 1		
1928	Jan 1			1929	Jan 1		
1930	Jan 1			1931	Jan 1		
1932	Jan 1			1933	Jan 1		
1934	Jan 1			1935	Jan 1		
1936	Jan 1			1937	Jan 1		
1938	Jan 1			1939	Jan 1		
1940	Jan 1			1941	Jan 1		
1942	Jan 1			1943	Jan 1		
1944	Jan 1			1945	Jan 1		
1946	Jan 1			1947	Jan 1		
1948	Jan 1			1949	Jan 1		
1950	Jan 1			1951	Jan 1		
1952	Jan 1			1953	Jan 1		
1954	Jan 1			1955	Jan 1		
1956	Jan 1			1957	Jan 1		
1958	Jan 1			1959	Jan 1		
1960	Jan 1			1961	Jan 1		
1962	Jan 1			1963	Jan 1		
1964	Jan 1			1965	Jan 1		
1966	Jan 1			1967	Jan 1		
1968	Jan 1			1969	Jan 1		
1970	Jan 1			1971	Jan 1		
1972	Jan 1			1973	Jan 1		
1974	Jan 1			1975	Jan 1		
1976	Jan 1			1977	Jan 1		
1978	Jan 1			1979	Jan 1		
1980	Jan 1			1981	Jan 1		
1982	Jan 1			1983	Jan 1		
1984	Jan 1			1985	Jan 1		
1986	Jan 1			1987	Jan 1		
1988	Jan 1			1989	Jan 1		
1990	Jan 1			1991	Jan 1		
1992	Jan 1			1993	Jan 1		
1994	Jan 1			1995	Jan 1		
1996	Jan 1			1997	Jan 1		
1998	Jan 1			1999	Jan 1		
2000	Jan 1			2001	Jan 1		
2002	Jan 1			2003	Jan 1		
2004	Jan 1			2005	Jan 1		
2006	Jan 1			2007	Jan 1		
2008	Jan 1			2009	Jan 1		
2010	Jan 1			2011	Jan 1		
2012	Jan 1			2013	Jan 1		
2014	Jan 1			2015	Jan 1		
2016	Jan 1			2017	Jan 1		
2018	Jan 1			2019	Jan 1		
2020	Jan 1			2021	Jan 1		
2022	Jan 1			2023	Jan 1		
2024	Jan 1			2025	Jan 1		
2026	Jan 1			2027	Jan 1		
2028	Jan 1			2029	Jan 1		
2030	Jan 1			2031	Jan 1		
2032	Jan 1			2033	Jan 1		
2034	Jan 1			2035	Jan 1		
2036	Jan 1			2037	Jan 1		
2038	Jan 1			2039	Jan 1		
2040	Jan 1			2041	Jan 1		
2042	Jan 1			2043	Jan 1		

Sub 21.1
21.1 disca

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SUB E' $\begin{matrix} 1 \\ 2 \end{matrix}$

The apparatus
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Sub 33.
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4 and at least one switch, wherein the at least one service module comprises at
5 least one slave bidirectional FIFO unit, and wherein the at least one cell bus
6 controller comprises at least one master bidirectional FIFO unit.

1 34. A network switch platform comprising:

2 at least one service module;

3 at least one cell bus controller coupled among the at least one service
4 module and at least one switch;

5 at least one bidirectional first-in-first-out (FIFO) unit located in the at
6 least one service module and the at least one cell bus controller, wherein each
7 bidirectional FIFO unit comprises a first and a second unidirectional FIFO
8 buffer, wherein a cell size of the first and second unidirectional FIFO buffers is
9 programmable;

10 at least one diagnostic interface, wherein the at least one diagnostic
11 interface supports a non-destructive read of the at least one bidirectional FIFO
12 unit while at least one cell is being written to and read from the at least one
13 bidirectional FIFO unit; and

14 at least one discard enable signal, wherein at least one invalid cell can
15 be discarded from the at least one bidirectional FIFO unit using the at least
16 one discard enable signal.

1 35. The network switch platform of claim 34, wherein the at least one
2 bidirectional FIFO unit is coupled to write at least one cell from and read at
3 least one cell to at least one asynchronous transfer mode (ATM) interface, at
4 least one frame relay interface, at least one voice interface, and at least one
5 data interface.

1 36. The network switch platform of claim 34, wherein the at least one cell
2 is written to the second unidirectional FIFO buffer from the first
3 unidirectional FIFO buffer over a first enabled diagnostic loop, wherein at
4 least one cell is written to the first unidirectional FIFO buffer from the second
5 unidirectional FIFO buffer over a second enabled diagnostic loop.

1 37. The network switch platform of claim 34, wherein each unidirectional
2 FIFO buffer outputs a write port cell count, wherein a write port of each
3 unidirectional FIFO buffer outputs a status indicating space available in the
4 unidirectional FIFO buffer for at least one more cell, wherein each
5 unidirectional FIFO buffer outputs a read port cell count, wherein a read port
6 of each unidirectional FIFO buffer outputs a status indicating space available
7 in the unidirectional FIFO buffer for at least one more cell.

1 38. The network switch platform of claim 34, wherein the first and second
2 unidirectional FIFO buffers each comprise asynchronous read and write ports,
3 wherein the write port logic of each unidirectional FIFO buffer is
4 synchronous with a write clock, and wherein the read port logic of each
5 unidirectional FIFO buffer is synchronous with a read clock.

1 39. The network switch of claim 34, wherein a word size of the first and
2 second unidirectional FIFO buffers is programmable.

1 40. The network switch platform of claim 34, wherein the at least one
2 bidirectional FIFO unit is coupled to read at least one cell to and write at least
3 one cell from the at least one switch, wherein the switch handles cells from
4 sources having a plurality of bandwidths.

41. The network switch platform of claim 34, wherein the at least one service module is coupled to receive at least one cell from and provide at least one cell to at least one service subscriber using T1, E1, T3, E3, OC3, and OC 12 ports.

42. A method for controlling cell traffic in a switch platform, the method comprising the step of transferring at least one cell among a plurality of ports having a plurality of bandwidths using a bidirectional first-in-first-out (FIFO) unit, wherein the bidirectional FIFO unit comprises a first and a second unidirectional FIFO buffer having a programmable cell size.

43. The method of claim 42, further comprising the step of programming the word size of each of the first and second unidirectional FIFO buffers.

44. The method of claim 42, wherein the step of transferring comprises the steps of:
synchronously writing the at least one cell from at least one port to the first unidirectional FIFO buffer; and
synchronously reading the at least one cell from the first unidirectional FIFO buffer to at least one switch, wherein the reading is asynchronous with the writing.

45. The method of claim 42, wherein the step of transferring comprises the steps of:
synchronously writing the at least one cell from at least one switch to the second unidirectional FIFO buffer; and

5 synchronously reading the at least one cell from the second
6 unidirectional FIFO buffer to the at least one port, wherein the reading is
7 asynchronous with the writing.

1 46. The method of claim 42, further comprising the steps of:
2 discarding at least one invalid cell from each unidirectional FIFO
3 buffer; and
4 executing a non-destructive read of the at least one bidirectional FIFO
5 unit while at least one cell is being written to and read from the at least one
6 bidirectional FIFO.

1 47. The method of claim 42, further comprising the steps of:
2 writing at least one cell to the second unidirectional FIFO buffer from
3 the first unidirectional FIFO buffer using a first enabled diagnostic loop; and
4 writing at least one cell to the first unidirectional FIFO buffer from the
5 second unidirectional FIFO buffer over a second enabled diagnostic loop.

1 48. The method of claim 42, further comprising the steps of:
2 outputting a write port cell count from each unidirectional FIFO buffer;
3 outputting from a write port of each unidirectional FIFO buffer a status
4 indicating space available in the unidirectional FIFO buffer for at least one
5 more cell;
6 outputting a read port cell count from each unidirectional FIFO buffer;
7 and
8 outputting from a read port of each unidirectional FIFO buffer a status
9 indicating space available in the unidirectional FIFO buffer for at least one
10 more cell.

1 49. The method of claim 42, wherein the plurality of ports comprise at
2 least one asynchronous transfer mode (ATM) interface, at least one frame
3 relay interface, at least one voice interface, at least one data interface, at least
4 one network switch interface, at least one OC12 interface, and at least one OC3
5 interface.

add c⁴

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